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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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32294	7590	10/16/2008	EXAMINER	
SQUIRE, SANDERS & DEMPSEY L.L.P.			AGHDAM, FRESHTEH N	
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14TH FLOOR			ART UNIT	PAPER NUMBER
VIENNA, VA 22182-6212			2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,626	PAN ET AL.	
	Examiner	Art Unit	
	FRESHTEH N. AGHDAM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 September 2008.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,4,6-11,14 and 16-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,4,6-11,14, and 16-19 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Response to Arguments

Applicant's arguments filed September 9, 2008 have been fully considered but they are not persuasive.

Applicant's Arguments:

Regarding claims 1, 10, and 11, page 9, the applicant argues that the office action has failed to provide a prima facie case for obviousness "the Office Action failed to provide any reasoning for why a person of ordinary skill in the art would be motivated to combine Pikkarainen and Lipka."

Regarding claims 1, 10, and 11, pages 9-10, the applicant argues that the claimed subject matter is not taught or suggested by the combination of Pikkarainen and Lipka "wherein the performing of the delta sigma modulation comprises performing 2nd order delta sigma modulation to output 4 bits from a 10 bit input."

Examiner's Response:

Regarding the first argument set forth above, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the examiner provided a reason to combine in the previous office action dated July 9, 2008.

Regarding the second argument set forth above, the examiner disagrees with the applicant because in the previous office action dated July 9, 2008 the recited limitation is addressed, which is as follow:

Regarding the argument set forth above, the examiner disagrees with the applicant because (considering Pikkarainen employs a 1st order delta sigma modulator) one of ordinary skill in the art would recognize that using a second order delta sigma modulation is merely a matter of design choice and would have been obvious in the system of Pikkarainen because the higher the order of the delta sigma modulator the less the quantization noise (i.e. the higher the signal to noise ratio). In addition, one of ordinary skill in the art would recognize that reducing the number of bits of the digital quadrature signal from 10 bits to 4 bits at the output of the delta sigma modulator is merely a matter of design requirement and it would have been obvious in the system of Pikkarainen reduction of the number of bits from 10 bits to 4 bits because using a digital to analog converter with a higher bit width makes it possible to use a lower oversampling factor, which has a positive effect on the power consumption and depending on what the limit is for power consumption in that particular design the bit width could vary as it is evidenced by Lipka (Col. 2, lines 45-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 8, 10-14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikkarainen et al (US 5,701,106), and further in view of Lipka (US 7,227,910).

As to claims 1 and 10, Pikkarainen discloses a method of and/ or apparatus for modulating digital signal to higher frequency analog signal comprising: performing delta sigma modulation on a digital baseband quadrature signal (Fig. 8, block 91); converting the modulated signal to an analog signal (block 92); converting the analog signal to an RF signal (Col. 1, lines 13-18; Col. 4, lines 7-8); and inherently transmitting the RF signal. Furthermore, Pikkarainen discloses that the sigma delta modulation includes 1st or 5th order delta sigma modulation (Col. 5, lines 27-31) and the reduction is from n-bits to 1 bit. Pikkarainen does not expressly disclose the sigma delta modulation includes 2nd order delta sigma modulation that reduces the number of bits from 10 bits to 4 bits. However, one of ordinary skill in the art would recognize that using a second order delta sigma modulation is merely a matter of design choice and would have been obvious in the system of Pikkarainen because the higher the order of the delta sigma modulator the less the quantization noise (i.e. the higher the signal to noise ratio). Therefore, using a 2nd order delta sigma modulator and not for instance a 1st order delta sigma modulator will result in higher signal to noise ratio. It would have been obvious to one of ordinary skill in the art to use a 2nd order delta sigma modulator for the reason stated above. Also, One of ordinary skill in the art would recognize that reducing the number of bits of the digital quadrature signal from 10 bits to 4 bits at the output of the delta sigma

modulator is merely a matter of design requirement and it would have been obvious in the system of Pikkarainen reducing the number of bits from 10 bits to 4 bits because using a digital to analog converter with a higher bit width makes it possible to use a lower oversampling factor, which has a positive effect on the power consumption and depending on what the limit is for power consumption in that particular design the bit width could vary as it is evidenced by Lipka (Col. 2, lines 45-53). Therefore, it would have been obvious to one of ordinary skill in the art to reduce the number of bits from 10 to 4 for the reason stated above.

As to claims 4 and 14, Pikkarainen discloses all the subject matter claimed above, except for amplifying the RF signal prior to transmission. However, one of ordinary skill in the art would recognize that it is well known in the art to amplify the signal prior to transmission as it is evidenced by Lipka (Fig. 1, block 13) in order to adjust the signal gain prior to transmission as consequently improving the communication system performance.

As to claims 8 and 18, Pikkarainen discloses performing interpolation filtering on the digital quadrature signal before the delta sigma modulation (block 90).

As to claims 11, Pikkarainen discloses a method of and/ or apparatus for modulating digital signal to higher frequency analog signal comprising: performing delta sigma modulation on a digital baseband quadrature signal (Fig. 8, block 91); converting the modulated signal to an analog signal (block 92); converting the analog signal to an RF signal (Col. 1, lines 13-18; Col. 4, lines 7-8); and inherently transmitting the RF signal. Pikkarainen is not explicit about using a mixer to up convert the analog signal to

the RF signal. However, one of ordinary skill in the art would recognize that it is well known in the art to up utilize a mixer in order to up convert the intermediate signal to the RF signal to transmit the signal through radio frequency medium. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a mixer to up convert the signal to the RF signal for the reason stated above. Pikkarainen further does not expressly disclose the sigma delta modulation includes 2nd order delta sigma modulation that reduces the number of bits from 10 bits to 4 bits. However, one of ordinary skill in the art would recognize that using a second order delta sigma modulation is merely a matter of design choice and would have been obvious in the system of Pikkarainen because the higher the order of the delta sigma modulator the less the quantization noise (i.e. the higher the signal to noise ratio). Therefore, using a 2nd order delta sigma modulator and not for instance a 1st order delta sigma modulator will result in higher signal to noise ratio. It would have been obvious to one of ordinary skill in the art to use a 2nd order delta sigma modulator for the reason stated above. Also, One of ordinary skill in the art would recognize that reducing the number of bits of the digital quadrature signal from 10 bits to 4 bits at the output of the delta sigma modulator is merely a matter of design requirement and it would have been obvious in the system of Pikkarainen reducing the number of bits from 10 bits to 4 bits because using a digital to analog converter with a higher bit width makes it possible to use a lower oversampling factor, which has a positive effect on the power consumption and depending on what the limit is for power consumption in that particular design the bit width could vary as it is evidenced by Lipka (Col. 2, lines 45-53). Therefore, it would

have been obvious to one of ordinary skill in the art to reduce the number of bits from 10 to 4 for the reason stated above.

Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikkarainen et al and Lipka, further in view of Hossack (US 6,819,276).

As to claims 6 and 16, Pikkarainen and Lipka disclose all the subject matter claimed in claim 1, except for coding the modulated signal with a thermometer code. Hossack discloses a digital to analog converter that performs coding the modulated signal with a thermometer code (Fig. 3, block 120). Therefore, it would have been obvious to one of ordinary skill in the art to code the modulated signal with a thermometer code as Hossack discloses in order to reduce the number of bits that are in error.

Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikkaraninen et al and Lipka, and further in view of Norsworthy et al (US 5,512,898).

As to claims 7 and 17, Pikkarainen discloses modulating the quadrature signal using one of frequency shift keying and phase shift keying (Col. 2, lines 1-12). One of ordinary skill in the art would recognize that it is obvious to use different order frequency shift keying and phase shift keying modulations based on the channel state or design requirements. Pikkarainen and Lipka do not expressly disclose modulating the quadrature signal prior to performing delta sigma modulation. Norsworthy discloses modulating the quadrature signal using one of the frequency shift keying or phase shift

keying modulations prior to delta sigma modulation in order to highly efficiently transferring data by utilizing an I/Q modulation technique (Fig. 2, blocks 130 and 150; Col. 6, lines 7-11; Col. 10, lines 4-16). Therefore, it would have been obvious to one of ordinary skill in the art to perform I/Q modulation prior to delta sigma modulation for the reason stated above.

Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikkaraninen et al and Lipka, further in view of Fujimori (US 6,236,912).

As to claims 9 and 19, Pikkarainen and Lipka disclose all the subject matter claimed in claim 8, except for the interpolation filtering reduces the digital quadrature signal from 12 bits to 10 bits. Fujimori discloses that the interpolation filtering is capable of reducing the bit width by the interpolation rate change switch within the interpolation filter (Col. 6, lines 45-52). One of ordinary skill in the art would recognize that the exact value the bit width is a design requirement. Therefore, it would have been obvious to one of ordinary skill in the art to output a reduced bit width signal by the interpolation filter of Pikkaraninen as taught by Fujimori in order to reduce the hardware complexity of the device/ circuitry.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRESHTEH N. AGHDAM whose telephone number is (571)272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Freshteh N Aghdam/

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611